University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Lab Schedule

Week 1: 6/22/2009

Introduction to Lab Equipment and Software

Week 2: 6/29/2009

Lab 1 check-in
(Lab 1: Basic Combinational Logic Design with Seven-Segment Display)
[Lab # 1 Pre-lab due]

Week 3: 7/6/2009

Lab 1 continues

Week 4: 7/13/2009

Lab 1 check-out; Lab 2 check-in.
(Lab 2: 4-bit Adder Design: Verilog, Simulation, download to FPGA.)
[Lab # 2 Pre-lab due]

Week 5: 7/20/2009

Lab 2 check-out; Lab 3 check-in
(Lab 3: Counter Design)
[Lab # 3: No pre-lab due]

Week 6: 7/27/2009

Lab 3 check-out
Lab 4 check-in
(Lab 4: Thunderbird FSM design; ModelSim simulation; download to FPGA; software/hardware interface for testing)
[For Lab 4: Read the entire lab handout before coming to the lab.]

Week 7: 8/3/2009

Lab 4 continues
[Lab 4: Part 1 is due]

Week 8: 8/10/2009

Lab 4 check-out; Lab 5 check-in
(Lab 5: General-purpose FSM; RAM-based design.)
[Lab # 4 Check-out: Parts 2, 3 and 4 due]
[For Lab 5: Read Ch 8.5 (Serial Adder) in textbook]

Week 9: 8/17/2009

Lab 5 continues
[Lab 5: Parts 1 and 2 due]

Week 10: 8/24/2009

Lab 5 Check-out: Parts 3 and 4 due.